Amendments to the Claims

1. (Currently Amended) A method for generating a delay time by a processor system, comprising:

determining a number of loops value associated with a delay time and at least one characteristic value associated with a counter, wherein the number of loops value represents a number of counter rollover events;

storing the number of loops value in a memory;

determining a count value based on the number of loops value, wherein the count value is representable by the counter; ~~and~~

obtaining a current count value from the counter using a count reader and performing a comparison based on the current count value and a previous count value at least a number of times equal to the number of loops value; and

generating the delay time with the counter based on the number of loops value and the count value.

2. (Cancelled)

3. (Currently Amended) A method as defined in ~~claim 2~~ claim 1, further comprising determining that the delay time has been reached based on the comparison.

4. (Currently Amended) A method as defined in ~~claim 2~~ claim 1, wherein obtaining the current count value comprises reading a running count value of the counter.

5. (Original) A method as defined in claim 1, further comprising obtaining an initial count value.

6. (Original) A method as defined in claim 5, wherein determining the number of loops value comprises determining the number of loops value based on at least the initial count value.

7. (Previously Presented) A method as defined in claim 5, wherein determining the count value comprises determining the count value based on at least the initial count value.

8. (Original) A method as defined in claim 1, further comprising polling the counter.

9. (Original) A method as defined in claim 8, wherein polling the counter comprises polling the counter in a non-interrupt environment.

10. (Previously Presented) A method as defined in claim 1, wherein the at least one characteristic value is an amount of time required for the counter to count between a minimum count value of the counter and a maximum count value of the counter.

11. (Original) A method as defined in claim 1, wherein generating the delay time comprises generating the delay time prior to a boot process.

12. (Currently Amended) An apparatus for generating a delay time comprising:

a processor system including a memory; and

instructions stored in the memory that enable the processor system to:

determine a number of loops value associated with a delay time and at least one characteristic value associated with a counter, wherein the number of loops value represents a number of counter rollover events;

store the number of loops value in at least one of the memory or a second memory;

determine a count value based on the number of loops value, wherein the count value is representable by the counter; ~~and~~

obtain a current count value and perform a comparison based on the current count value and a previous count value at least a number of times equal to the number of loops value; and

generate the delay time with the counter based on the number of loops value and the count value.

13. (Cancelled)

14. (Currently Amended) An apparatus as defined in ~~claim 13~~ claim 12, wherein the instructions stored in the memory enable the processor system to determine that the delay time has been reached based on the comparison.

15. (Original) An apparatus as defined in claim 12, wherein the instructions stored in the memory enable the processor system to obtain an initial count value.

16. (Original) An apparatus as defined in claim 15, wherein the instructions stored in the memory enable the processor system to determine the number of loops value based on at least the initial count value.

17. (Original) An apparatus as defined in claim 12, wherein the instructions enable the processor system to poll the counter in a non-interrupt environment.

18. (Previously Presented) An apparatus as defined in claim 12, wherein the at least one characteristic value is an amount of time required for the counter to count between a minimum count value of the counter and a maximum count value of the counter.

19. (Original) An apparatus as defined in claim 12, wherein the instructions enable the processor system to generate the delay time prior to a boot process.

20. (Previously Presented) An apparatus as defined in claim 12, wherein the memory is at least one of a flash memory or a read only memory.

21. (Currently Amended) A system for generating a delay time comprising:

a counter;

a count reader to obtain count values from ~~a~~ the counter;

a comparator communicatively coupled to the count reader and to perform comparisons based on at least some of the count values;

a loop counter communicatively coupled to the comparator and to modify a number of loops value stored in a memory based on at least some of the comparisons, wherein the number of loops value represents a number of counter rollover events associated with a delay time and at least one characteristic value associated with the counter, ~~and~~ wherein the system generates a delay time based on the comparisons, the number of loops value, and the at least some of the count values by obtaining a current count value of the counter via the count reader, performing a comparison via the comparator based on the current count value and a previous count value at least a number of times equal to the number of loops value, and wherein at least one of the counter, the count reader, the comparator, and the loop counter is implemented using a hardware circuit.

22. (Previously Presented) A system as defined in claim 21, wherein the count reader is further to obtain an initial count value.

23. (Previously Presented) A system as defined in claim 22, further comprising a value generator that is to generate at least one of the count values and the number of loops value based on the initial count value.

24. (Cancelled)

25. (Cancelled)

26. (Previously Presented) A system as defined in claim 21, wherein the counter is at least one of a non-resetable counter or a non-resetable timer.

27. (Previously Presented) A system as defined in claim 21, wherein the system is to generate the delay time in a non-interrupt environment.

28. (Previously Presented) A system as defined in claim 21, wherein the system is to generate the delay time prior to a boot phase.

29. (Currently Amended) A computer readable medium having instructions stored thereon that, when executed, cause a machine to:

determine a number of loops value associated with a delay time and at least one characteristic value associated with a counter, wherein the number of loops value represents a number of counter rollover events;

store the number of loops value in a memory;

determine a count value based on the number of loops value, wherein the count value is representable by the counter; ~~and~~

obtain a current count value and perform a comparison based on the current count value and a previous count value at least a number of times equal to the number of loops value; and

generate the delay time with the counter based on the number of loops value and the count value.

30. (Cancelled)

31. (Currently Amended) A computer readable medium as defined in ~~claim 30~~ claim 29 having instructions stored thereon that, when executed, cause the machine to determine that the delay time has been reached based on the comparison.

32. (Original) A computer readable medium as defined in claim 29 having instructions stored thereon that, when executed, cause the machine to obtain an initial count value.

33. (Original) A computer readable medium as defined in claim 32 having instructions stored thereon that, when executed, cause the machine to determine the number of loops value based on at least the initial count value.

34. (Previously Presented) A computer readable medium as defined in claim 32 having instructions stored thereon that, when executed, cause the machine to determine the count value based on at least the initial count value.

35. (Original) A computer readable medium as defined in claim 29 having instructions stored thereon that, when executed, cause the machine to poll the counter.

36. (Original) A computer readable medium as defined in claim 29 having instructions stored thereon that, when executed, cause the machine to poll the counter in a non-interrupt environment.

37. (Original) A computer readable medium as defined in claim 29 having instructions stored thereon that, when executed, cause the machine to decrement the number of loops value based on at least one rollover event of the counter.

38. (Original) A computer readable medium as defined in claim 29 having instructions stored thereon that, when executed, cause the machine to generate the delay time prior to a boot process.

39. (Currently Amended) An apparatus for generating a delay time comprising:

a processor system including a flash memory; and

instructions stored in the flash memory that enable the processor system to:

determine a number of loops value associated with a delay time and at least one characteristic value associated with a counter, wherein the number of loops value represents a number of counter rollover events;

store the number of loops value in at least one of the flash memory or a second memory;

determine a count value based on the number of loops value, wherein the count value is representable by the counter; ~~and~~

obtain a current count value and performing a comparison based on the current count value and a previous count value at least a number of times equal to the number of loops value; and

generate the delay time with the counter based on the number of loops value and the count value.

40. (Original) An apparatus as defined in claim 39, wherein the instructions enable the processor system to generate the delay time prior to a boot process.

Please add the following new claims

41. (New) A method as defined in claim 1, wherein generating the delay time comprises generating the delay time in a pre-boot environment without the use of interrupts.

42. (New) An apparatus as defined in claim 12, wherein the instructions enable the processor system to generate the delay time in a pre-boot environment without the use of interrupts.

43. (New) A system as defined in claim 21, wherein the system is to generate the delay time in a pre-boot environment without the use of interrupts.

44. (New) A computer readable medium as defined in claim 29 having instructions stored thereon that, when executed, cause the machine to generate the delay time in a pre-boot environment without the use of interrupts.

45. (New) An apparatus as defined in claim 39, wherein the instructions enable the processor system to generate the delay time in a pre-boot environment without the use of interrupts.